The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) An apparatus, comprising;

an active semiconductor layer;

a transistor formed in the active silicon layer;

a bulk silicon layer having a first surface and a second surface;

an oxide layer formed between the active silicon layer and the first surface of the bulk silicon layer; and

a heat sink formed in the bulk silicon layer and configured to sink heat sourced through the oxide layer to the second surface of the bulk silicon layer, the heat sink being a thermally conductive material provided in the bulk silicon layer, the thermally conductive material being a thermally conductive paste.

2. (cancelled)

3. (cancelled)

4. (cancelled)

5. (cancelled)

6. (original) The apparatus of claim 1, wherein the transistor is an MOS transistor.

7. (original) The apparatus of claim 1, wherein the transistor is a bipolar transistor.

8. (original) The apparatus of claim 1, further comprising isolation regions formed around the transistor in the active silicon layer and contacting the oxide layer formed between the active silicon layer and the first surface of the bulk silicon layer.

9. (original) The apparatus of claim 1, wherein the heat sink is substantially plug shaped.

10. (original) The apparatus of claim 9, wherein the plug has a length substantially the same as the thickness of the bulk silicon layer.

11. (original) The apparatus of claim 9, wherein the plug has a circumference ranging from 1 to 50000 microns.

12. (previously presented) The apparatus of claim 1, further comprising

a plurality of transistors formed in the active region, and

a plurality of heat sinks associated with the plurality of transistors respectively, each of the plurality of heat sinks formed in the bulk silicon layer configured to sink heat sourced in the oxide layer to the second surface of the bulk silicon layer, each of the heat sinks being plugged shaped and filled with the thermally conductive paste.

13. (original) The apparatus of claim 12, wherein the plurality of transistors and the plurality of heat sinks are formed on a semiconductor die.

14. (original) The apparatus of claim 12, wherein the plurality of transistors and the plurality of heat sinks are formed on a semiconductor wafer.

15. (original) The apparatus of claim 1, wherein the bulk silicon layer is formed in a semiconductor material having one of the following orientations: 100, 111, or 110.

16. (original) The apparatus of claim 1, wherein the active silicon layer is formed in a semiconductor material having one of the following orientations: 100, 111, or 110.

17. -25. (cancelled)

26. (previously presented) The apparatus of claim 1, wherein the thermally conductive paste is DAG.